CSS555(C) Micropower Timer (SPICE Model)

Overview

The analog section of the CSS555 (and CSS555C) contains a micro-power version of the standard 555 Timer. It is designed in an advanced CMOS process and includes programmable options so it can be configured to fit the intended application. Speed, power, trip levels and counter settings are stored in an internal EEPROM.

To assist board level design, a SPICE model for CSS's 555 Timer has been developed. It provides a simulation capability at the component level. To make it portable across many simulators, it uses only Level 1 device models. The comparators are modeled with BLM gain blocks to reduce simulation time. Even with these simplifications, the model provides a very good representation of the real IC.

The CSS 555 Timer model includes:

1) Supply Current (over V_{DD})
2) Input Switch Levels
3) Propagation Delay Time
4) Output Drive (over temperature and V_{DD})
5) ESD Clamp Diodes and Pad Capacitance

The power and trip level settings change the IC's supply current, propagation delay and trip level parameters. Separate SPICE model files are provided for each combination of power and trip level settings. The table shown below (Table 1) lists the available models.

Power Setting	Trip Levels	SPICE Model	
		CSS555	CSS555C
Micro	Standard	CSS555_uPwr_StdLev	CSS555C_uPwr_StdLev
Micro	Low Voltage	CSS555_uPwr_LowVLev	CSS555C_uPwr_LowVLev
Low	Standard	CSS555_LowPwr_StdLev	CSS555C_LowPwr_StdLev
Low	Low Voltage	CSS555_LowPwr_LowVLev	CSS555C_LowPwr_LowVLev

Table 1

Block Diagram

A simplified block diagram of a 555 timer is shown, for reference, in Figure 1.

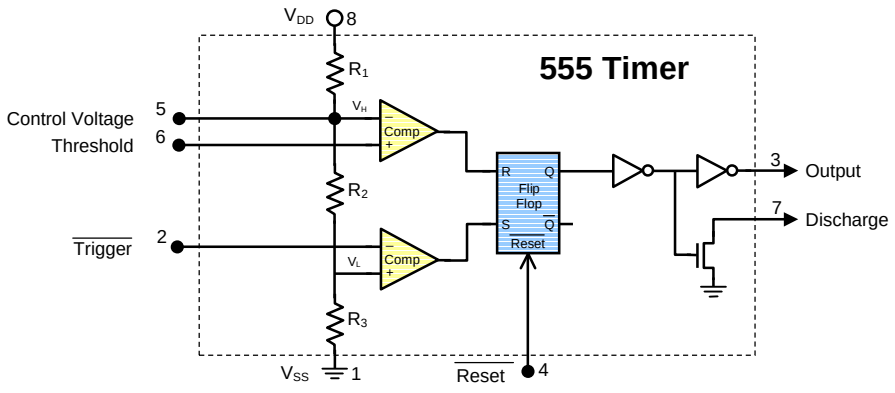

Figure 1

CSS555 SPICE Model

The CSS555 SPICE model has been structured to provide an accurate model that runs quickly and is compatible with most SPICE simulators. It includes the analog portion of the IC and covers most of the important electrical characteristics, including supply current, input levels, output drive and propagation delay. The model can be used over a wide operating range: V_{DD} = 1.2V to 5.5V, Temperature = -40℃ to +85℃. Most of the device parameters are valid acr oss this range. Models for different configuration settings (power & trip levels) are also provided, along with tables to adjust the models for worst-case conditions. A summary of the functions and parameters included in the model is shown in Table 2. A schematic of the model is provided in Appendix A.

Model Summary

Parameter/Function	Symbol	Description	Components
Supply Current	I_{DD0}	Supply current (Standby mode)	R3, R4, R5, IBIAS, RBIAS, D8 (A/B/C)
Reset Input Levels	V_{RST}	CMOS input switch level	MP4, MN4, Level 1 models
Trip Levels	V_{TRIG}, V_{CTRL}	Resistor divider (1/3, 2/3 or 10%, 90% of V_{DD})	R3, R4, R5
Input Comparators Voltage limiters		Ideal voltage gain blocks RC + Diode clamps	EC1, EC2 (A_V = 1000) R1, DL1P, DL1N & R2, DL2P, DL2N
RS Flip Flop		CMOS NOR Gates (NOR2 & NOR3) RC delay in feedback path	Level 1 MOSFET models RNR2D, CNR2D, RNR3D, CNR3D
Delay Time	t_{DLY}	Delay from TRIG/VT inputs to Timer Output	R1, CD1; R2, CD2; RDLY, CDLY
Timer Output Driver	V_{OL}, V_{OH}	CMOS output driver	MP3, MN3, Level 1 models
Discharge Output	V_{DIS}	Open drain output	MN7, Level 1 model
ESD Clamp Diodes		Input protection diodes, Pins 2 - 7	DN2 – DN7, DP2 – DP7

Note: Component and model values are centered for operation at 3.0V, 25℃

Table 2

Supply Current (IDD0)

The static supply current is made up of three components: the trip level resistor divider, the comparators and the bias current generator (for the comparators). The first component is linearly proportional to the supply voltage and modeled by the divider (R3, R4, & R5). The last two components are lumped together and modeled by a DC current source (IBIAS) and a resistor (RBIAS) across the supply. Diodes D8A, D8B and D8C have been included to shunt IBIAS to V_{SS} when V_{DD} is less than 0.5V. The values of IBIAS and RBIAS depend on the power setting. This relatively simple model provides a reasonably accurate model of the static supply current for supply voltages from 0V to 5.5V.

The bias current generator is temperature compensated to keep the comparator speed relatively constant over temperature. Since the supply current is a weak function of temperature (and not linear), the CSS555 model does not include a temperature coefficient for I_{DD0}.

For most applications, the transient or switching current is a small component of the total current. The RS flip-flop and output driver are included in this component. The current required to drive off-chip devices is often the dominant component of the switching current and is included in the model by way of the output driver (MOSFET MP3).

Reset Input

The Reset input drives a CMOS inverter. It is modeled by MP4 and MN4. The ratio of the Pch and Nch W/L's provide a switch level of approximately ½ x V_{DD}. Input leakage current (I_L) in the real device is typically less than 1nA and can be positive or negative. Since I_L is typically negligible and may be either polarity, it is not included in the model.

Trip Levels (V_{CTRL} & V_{TRIG})

The standard upper and lower trip levels are ⅔ x V_{DD} and ⅓ x V_{DD}. They are generated by the resistor divider formed by R3, R4 and R5. To minimize power, each resistor is 2.5MΩ. To gain more "head room" for the comparators at low supply levels, the trip levels can be changed to 0.9 x V_{DD} and 0.1 x V_{DD}. For this configuration, R3, R4 and R5 are changed to 750KΩ, 6.0MΩ and 750KΩ respectively. (The total series resistance remains 7.5MΩ.)

CSS555 SPICE Model (continued)

Input Comparators

The input comparators are modeled with ideal gain elements (EC1 and EC2). They are "E" components with a voltage gain of 1000. (The real comparators use a folded-cascode topology and are operated in a sub-threshold region. Level 1 models are not very accurate for this region, so ideal gain blocks were used instead. The gain elements also provide a shorter simulation run time.) Each gain element is followed by a "Limiter" circuit. An RC filter (R_N, CD_N) limits the maximum slew rate and adds a small delay. Diodes (DLN_N & DLP_N) clamp the comparator output voltage if it goes below (V_{SS} – 0.5V) or above (V_{DD} + 0.5V).

RS Flip-Flop

The RS flip-flop is modeled by two cross-coupled CMOS NOR gates, just like the actual circuit. Its simulated speed, input levels and switching current are accurately modeled over supply voltage and temperature. The feedback paths include a 10ns RC delay to improve convergence.

Propagation Delay Time

The propagation delay from the timer input (TRIGGER or THRESHOLD) to the timer OUTPUT is dominated by the speed of the comparators. It is lumped into a single RC delay between the RS flip-flop and output driver. A more accurate location would place an RC delay circuit after each limiter. However, a slow signal driving a flip-flop input can cause convergence problems due to the feedback within the flip-flop. For that reason, the delay is located after the flip-flop. The down side to this location is the increased sensitivity to a narrow glitch at the inputs. The real circuit will filter out glitches that the model will respond to.

Output Drivers

The two outputs, "OUTPUT" and "DISCHARGE", are modeled with level 1 MOSFET's. Their drive strengths are automatically adjusted for both supply voltage and temperature. The models have been centered for operation at V_{DD} = 3.0V and 25℃. The drive strength of the OUTPUT pin is balanced. (Its sink and source currents are approximately equal.)

To check the model, force the output current to ±4mA with VDD = 3.0V and temperature = 25℃. The output voltage should be: V_{OL} ~ 152mV and V_{OH} ~ (V_{DD} - 145mV). At 85℃, the output voltage should be: V_{OL} ~ 185mV and V_{OH} ~ (V_{DD} - 175mV). (~20% increase in R_{ON}.)

In the real CSS555 IC, the output driver employs a "Break-Before-Make" pre-driver. This prevents the large current spikes that can occur if both output FET's are on during the switching time. The pre-driver delays the turn-on signal until the FET that was on turns completely off. For simplicity, the pre-driver is modeled with three cascaded inverters. It does not include the "Break-Before-Make" logic. Therefore the model will tend to overestimate the switching current. To make it more realistic, the first stage of the pre-driver is powered by "Buffered V_{DD}". Its switching current is not included with V_{DD}. The input signal to the pre-driver comes directly from the RC delay circuit and is very slow, which is not the case in the real circuit. The slow rise and fall times generate higher switching currents than what would be seen with the real circuit.

Input Protection Diodes and Pad Capacitance

Virtually all CMOS IC's have clamp diodes on their I/O pins to prevent damage due to ESD. Clamp diodes have been included in this model. If an I/O pin is forced above V_{DD} or below V_{SS}, the clamp diode will conduct heavily and limit the voltage at the pin. The diode's series resistance is about 5 ohms. Each pad has approximately 5pF capacitance to V_{SS}.

Convergence Errors

The feedback path in the RS flip-flop will occasionally cause convergence problems. If the circuit fails to converge, try the following:

1) Increase the "Transient Time Point Iteration Limit" (suggest at least 25)
2) Decrease the "Relative Accuracy"
3) Change the "Maximum Step Size" (suggest 1ns to 100ns)
4) Enable "GMIN Stepping" (if available)
5) Increase the supply voltage

CSS555 SPICE Model (continued)

Worst Case Models

The models supplied for the CSS555 device are "Typical" models. The model parameters are centered for an average device. It is fairly straightforward to modify the model for worst-case speed, power, delay and output drive conditions. These parameters are generally dominated by one or two components or process parameters. The following tables show the changes to the model to cover worst-case conditions. (The worst-case model parameters are based on statistical data for the CSS555 device and the wafer process. They are approximations. They represent a three-sigma variation based on available data.)

Micro-power, Standard Trip Levels

Parameter	Symbol	Components	Slow Speed Low Power	Typical	Fast Speed High Power
Supply Current	I_{DD0}	RBIAS, IBIAS	2.90MΩ, 1.0uA	2.25MΩ, 1.4uA	1.70MΩ, 1.9uA
Trip Levels	V_{TRIG}, V_{CTRL}	R3, R4, R5	3.0, 3.03, 3.0MΩ	2.5, 2.5, 2.5MΩ	2.0, 1.97, 2.0MΩ
Delay Time	t_{DLY}	RDLY, CDLY	2.4MΩ, 1pF	2.0MΩ, 1pF	1.6MΩ, 1pF
Timer Output Driver	V_{OL}, V_{OH}	MP3, MN3 (KP in model)	2.1E-5, 6.0E-5	2.6E-5, 7.0E-5	3.1E-5, 8.0E-5
Discharge Output	V_{DIS}	MN7 (KP in model)	6.0E-5	7.0E-5	8.0E-5

Table 3A

Low-power, Standard Trip Levels

Parameter	Symbol	Components	Slow Speed Low Power	Typical	Fast Speed High Power
Supply Current	I_{DD0}	RBIAS, IBIAS	520KΩ, 6.9uA	400KΩ, 9.3uA	300KΩ, 12.5uA
Trip Levels	V_{TRIG}, V_{CTRL}	R3, R4, R5	3.0, 3.03, 3.0MΩ	2.5, 2.5, 2.5MΩ	2.0, 1.97, 2.0MΩ
Delay Time	t_{DLY}	RDLY, CDLY	600KΩ, 1pF	500KΩ, 1pF	400KΩ, 1pF
Timer Output Driver	V_{OL}, V_{OH}	MP3, MN3 (KP in model)	2.1E-5, 6.0E-5	2.6E-5, 7.0E-5	3.1E-5, 8.0E-5
Discharge Output	V_{DIS}	MN7 (KP in model)	6.0E-5	7.0E-5	8.0E-5

Table 3B

Micro-power, Low Voltage Trip Levels

Parameter	Symbol	Components	Slow Speed Low Power	Typical	Fast Speed High Power
Supply Current	I_{DD0}	RBIAS, IBIAS	2.90MΩ, 1.0uA	2.25MΩ, 1.4uA	1.70MΩ, 1.9uA
Trip Levels	V_{TRIG}, V_{CTRL}	R3, R4, R5	0.60, 4.85, 0.60MΩ	0.75, 6.0, 0.75MΩ	0.90, 7.13, 0.90MΩ
Delay Time	t_{DLY}	RDLY, CDLY	2.4MΩ, 1pF	2.0MΩ, 1pF	1.6MΩ, 1pF
Timer Output Driver	V_{OL}, V_{OH}	MP3, MN3 (KP in model)	2.1E-5, 6.0E-5	2.6E-5, 7.0E-5	3.1E-5, 8.0E-5
Discharge Output	V_{DIS}	MN7 (KP in model)	6.0E-5	7.0E-5	8.0E-5

Table 3C

Low-power, Low Voltage Trip Levels

Parameter	Symbol	Components	Slow Speed Low Power	Typical	Fast Speed High Power
Supply Current	I_{DD0}	RBIAS, IBIAS	520KΩ, 6.9uA	400KΩ, 9.3uA	300KΩ, 12.5uA
Trip Levels	V_{TRIG}, V_{CTRL}	R3, R4, R5	0.60, 4.85, 0.60MΩ	0.75, 6.0, 0.75MΩ	0.90, 7.13, 0.90MΩ
Delay Time	t_{DLY}	RDLY, CDLY	600KΩ, 1pF	500KΩ, 1pF	400KΩ, 1pF
Timer Output Driver	V_{OL}, V_{OH}	MP3, MN3 (KP in model)	2.1E-5, 6.0E-5	2.6E-5, 7.0E-5	3.1E-5, 8.0E-5
Discharge Output	V_{DIS}	MN7 (KP in model)	6.0E-5	7.0E-5	8.0E-5

Table 3D

CSS555(C) Micropower Timer (SPICE Model)

CSS555 SPICE Model Schematic